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VHDL Design with FPGAs

Lab 1- Switch Count

CPE 3020 (01)

Code

library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

-- Uncomment the following library declaration if using

-- arithmetic functions with Signed or Unsigned values

--use IEEE.NUMERIC\_STD.ALL;

-- Uncomment the following library declaration if instantiating

-- any Xilinx leaf cells in this code.

--library UNISIM;

--use UNISIM.VComponents.all;

entity intro is

port (

--Switch inputs-------------------------------INPUTS

sw0: in std\_logic;

sw1: in std\_logic;

sw2: in std\_logic;

--LED Outputs--------------------------------OUTPUTS

led0: out std\_logic; --all LEDs are active low

led1: out std\_logic;

led2: out std\_logic

);

end intro;

architecture intro\_arch of intro is

begin

led0 <= not(sw0 or sw1 or sw2);

led1 <= not((sw0 and sw1) or (sw0 and sw2) or (sw1 and sw2));

led2 <= not(sw0 and sw1 and sw2);

end intro\_arch;

Block Diagram

SW1 LED1

SW2 LED2

SW3 LED3

Inputs Outputs